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THOMAS W. SIGMON
PRINCIPAL INVESTIGATOR
DEPARTMENT OF ELECTRICAL ENGINEERING
ARIZONA STATE UNIVERSITY
BOX 875706
TEMPE, AZ 85287-5706
SIGMON@ENUXSA.EAS.ASU.EDU
602-965-5580

DR. C. NEIL BERGLUND
TECHNICAL LIAISON
DEPARTMENT OF ELECTRICAL ENGINEERING AND APPLIED PHYSICS
OREGON GRADUATE INSTITUTE
P.O. BOX 91000 PORTLAND, OR 97291
20000 N.W. WALKER RD
BEAVERTON, OR 97006
503-690-1130

EVALUATION OF PULSED UV-LASER GAS PHASE DOPING FOR FABRICATION OF HIGH PERFORMANCE POLYSILICON TFTs

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800 NORTH QUINCY STREET
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EVALUATION OF PULSED UV-LASER GAS PHASE DOPING FOR FABRICATION OF HIGH PERFORMANCE POLYSILICON TFTs

I. SUMMARY

The primary purpose of this research effort is to investigate and characterize the use of Gas Immersion Laser Doping (GILD) for the fabrication of polysilicon TFTs. To achieve this goal we will be investigating the fabrication of poly-Si TFTs using both standard, industrially recognized doping and annealing processes in parallel with laser processing annealing. A TFT process flow was developed this quarter, and it has been applied to several experiments in which both conventional and laser processed NMOS TFTs were made. This process flow and the wafer splits that use it are briefly outlined in section II below. Section III concludes by stating future efforts.

II. TECHNICAL REPORT

During the first quarter's effort we have designed a process flow for the fabrication of simple TFTs and materials test structures useful for evaluation and comparison of conventionally processed versus laser processed polysilicon material. All experiments start with (100) 4" Si wafers having 4600 Å of thermal oxide. 1000 Å of LPCVD a-Si is then deposited on this oxide, and recrystallized by a 600°C furnace anneal in Ar for 18 hours. Table I and Fig. 1 identify the major splits in our processing and doping experiments.

Table I Wafer Split Variables for TFT Run 1

Number of Wafers	Ion Implant Gate	GILD S/D/G	Ion Implant S/D/G	Furn. Anneal S/D/G	Laser Anneal S/D/G
2	-	-	X	X	-
2	-	-	X	X	X
2	X	X	-	-	-

X = process this step - = skip this step

The condensed process flow, not listing cleans, etc. is listed below. Fig. 2 shows the completed TFT device cross section.

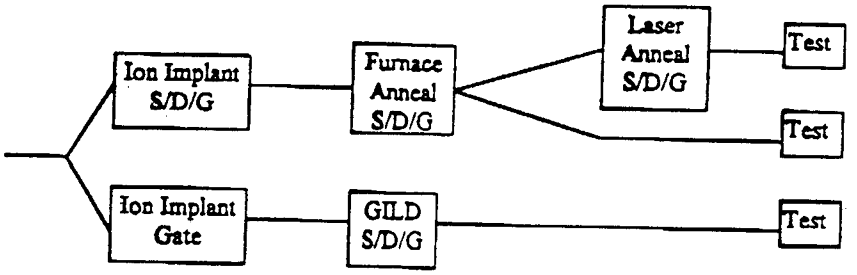

Fig. 1 Wafer Split for TFT Run 1

TFT Process Flow:

1. Grow 4600 Å thermal oxide
2. Deposit 1000 Å LPCVD a-Si
3. Furnace recrystallization at 600°C in Ar for 18 hours
4. Plasma etch polysilicon islands (device active area)
5. Deposit gate LTO, 1000 Å at 300°C
6. Deposit gate polysilicon, 3000 Å LPCVD at 600°C
7. (GILD Split) Implant Gate with $1x10^{15}$ cm^{-2} phosphorus at 60 keV
8. Plasma Etch Gate Pattern
9. (Ion Implant Split) Implant S/D/G with $1x10^{15}$ cm^{-2} phosphorus at 60 keV
10. Anneal implants, 600°C in Ar for 1 hour
11. Strip LTO (1st 700 Å using RIE, and last 300 Å using BOE)
12. (Ion Implant + Laser Anneal Split) Laser anneal S/D/G
13. (GILD Split) GILD process S/D/G
14. Deposit 6000 Å LTO at 300°C
15. Pattern contact windows
16. Open etch contact windows using 20:1 BOE
17. Sputter Al-Si 1% for contacts
18. Pattern contact level
19. Sinter at 400°C for 45 min. in forming gas
20. Electrical Testing

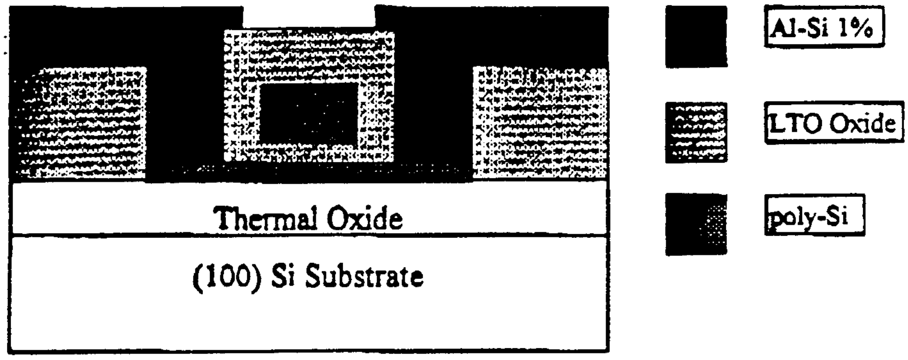

Fig. 2 Final TFT Device Cross Section

III. FUTURE EFFORT

This last quarter developed a working process for both conventionally and laser processed TFTs. We recently completed Run 1 of this process by fabricating NMOS TFTs. Next quarter's report will concentrate on the following:

i) Begin electrical testing of Run 1

ii) Use test results of Run 1 to re-evaluate and modify (if needed) the TFT Process Flow outlined above

iii) Plan TFT Process Run 2, based on Run 1 test results